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Dedicated Probe System for Wafer Level Noise Measurements in MOS Devices

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Abstract *- Noise measurements represent an interesting investigation technique for the characterization of the quality and reliability of microelectronic materials and devices. Performing meaningful noise measurements, however, may be quite challenging, particularly because of the many sources of interferences that superimpose to the noise signal. For this reason packaged samples are preferred because they allow accurate shielding from the external environment, and because keeping the sample in close proximity to the low noise biasing system and amplifier reduces microphonic and electromagnetic disturbances. Notwithstanding this, the possibility of performing noise measurements at wafer level would be quite interesting both because of the ease of obtaining wafer level samples from industries with respect to packaged samples, and because this would avoid possible packaging-process induced device degradation. The purpose of this work is to demonstrate that it is in fact possible to design and build a dedicated probe system for performing high sensitive noise measurements on MOS devices at wafer level.*

Keywords *- noise measurement, spectral analysis, wafer level measurement, MOS devices.*

I. INTRODUCTION

The evaluation of the current or voltage spontaneous fluctuations, commonly referred to as noise measurements, represents a fundamental investigation technique for the characterization of microelectronic materials and devices [1]. One of the most relevant applications of this technique is in the field of thin-oxide Metal-Oxide-Semiconductor (MOS) structures characterization. By using this kind of investigation, significant insights have been obtained in the understanding of the charge transport mechanisms and of the defects properties at different oxide degradation stages. As an example, it has been proposed that the observed $1/f$ noise is due to the superposition of several individual fluctuators consisting of electron traps inside the oxide or at the Si/SiO_2 interface [2]. Therefore, the evaluation of the $1/f$ noise can be used as a sensitive measure of the oxide traps and interface states densities. It has also been shown that the oxide breakdown is always preceded by random telegraph noise in the gate current [3]. Moreover, the partial reduction of the shot noise level in MOS structures after a high field stress has been used as a strong proof that the observed stress-induced leakage currents are due to trap-assisted tunneling [4]. Because of the presence of many interferences sources, it is normally quite difficult to perform meaningful noise measurements. In order to obtain accurate results, a suitable shielding from the external environment is necessary. Therefore, packaged samples are preferred because they allow having the sample in close proximity to the low noise biasing system and amplifier, thus reducing the effects of electromagnetic disturbances, which increase as the length of the cabling increases. In fact in the case of wafer level measurements, the large size of the probe station chamber would require long cables for connecting the DUT (Device Under Test) to the noise measurement system. Moreover such devices as the vacuum pump used to hold the wafer in place would introduce intolerable mechanical vibrations. Finally, in most cases, a considerable level of noise is generated at the point contact between the probe tips and the DUT pads. Notwithstanding these difficulties, it would be quite interesting to succeed in performing noise measurements at wafer level both because of the ease of obtaining wafer level samples from industries with respect to packaged samples, and because this would prevent possible packaging process induced device degradation. In the case of MOS structures, at least the problem of the tips contact noise, which is proportional to the square of the DC current, can be neglected because of the low conduction current which is normally observed when performing noise measurements [5]. In this paper we demonstrate that it is in fact possible to design and build a dedicated probe system for performing high sensitive noise measurements on MOS devices at wafer level.

II. PROPOSED APPROACH

As we have noted above, a close proximity between the DUT and the noise measurement system in a carefully shielded environment is essential for performing sensible noise measurements. For this reason, in view of the peculiarity of noise measurements with respect to other characterization techniques, we renounced to the possibility of realizing a probe system capable of hosting an entire today standard 8-inch wafer. The sample holder top plate is a circle with a diameter of 3 cm and can therefore host quite large dies as those used for containing several test structures. A schematic view of the system we have realized is reported in Fig. 1a, while Fig. 1b shows a photograph of the entire system. The entire structure of the system is obtained starting from two 4 mm thick

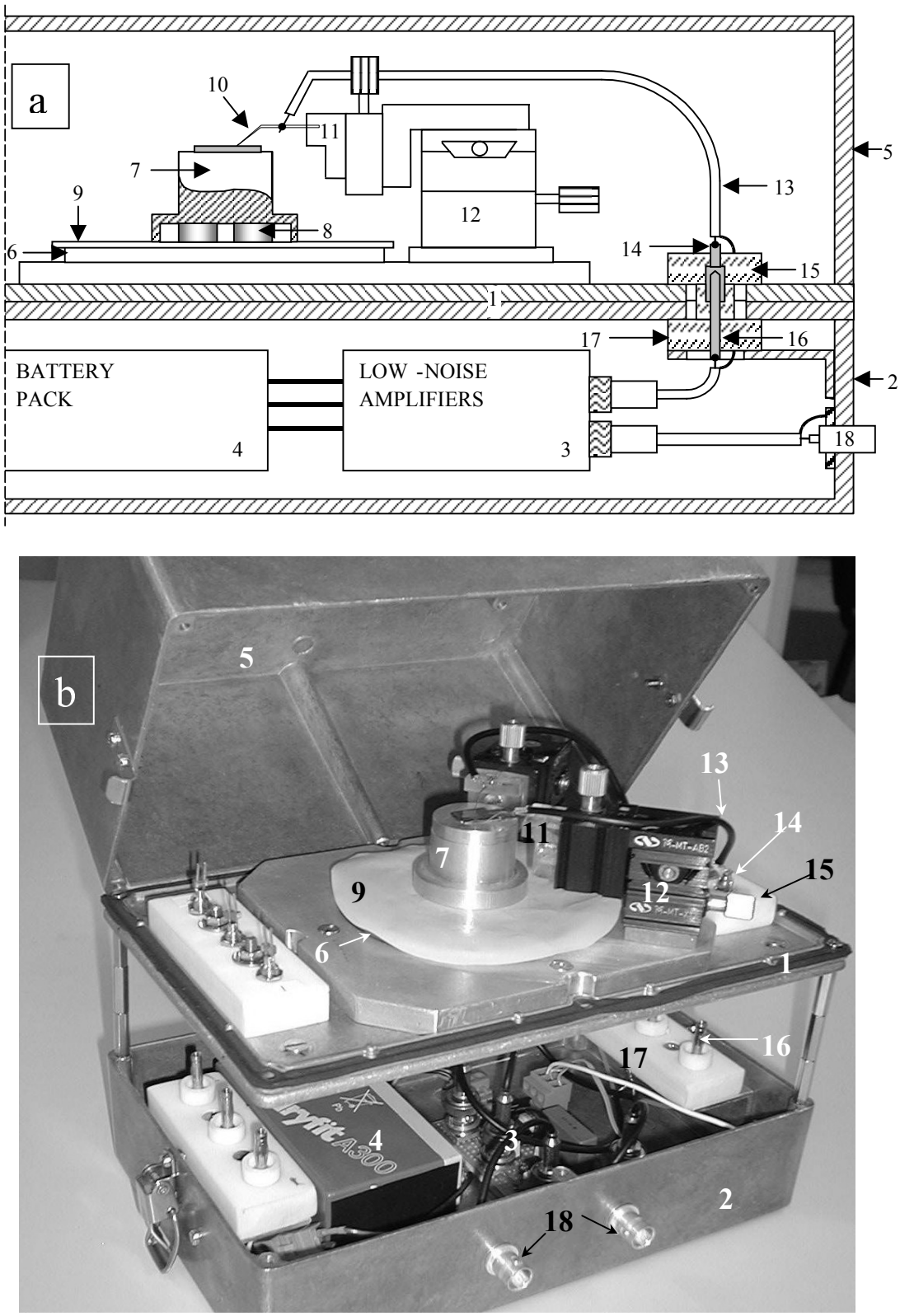

Fig. 1. Schematic view (a) and photograph (b) of the probe system for wafer level noise measurements.

aluminum boxes, the cover plates of both being screwed together to form the base (1), which is 14 cm×22 cm wide. One of the boxes is used to form the bottom section (2), which hosts the biasing system and the noise preamplifiers (3) together with the battery pack (4). The height of this section is 5 cm, but a taller box may be used in case more room is needed. The other box forms the top cover (5) and is 10 cm in height. A ferromagnetic flat base (6) is present on top of the base onto which the sample holder (7), which has four magnetic disks inserted in its base (8), can slide for a coarse positioning of the DUT within the contacting range of the probes. A thin (0.1 mm) PTFE foil (9) allows electrical insulation of the sample holder from the bulk of the probe system. Up to four probes can be hosted onto the base (only two of them are present in Fig. 1b) so that four contacts measurement configurations are possible. The probes consist of standard tungsten tips (10) embedded in an insulating holder (11) each of which is mounted on an XYZ precision translator (12). The inner conductor of a RG174 coaxial cable (13) is soldered to a miniature screw wire holder, which is secured to the tungsten tip of each probe. The other end of the cable is connected to a 4 mm female connector (14), which is inserted in a highly insulating PTFE holder (15), which, in turn, is screwed to the base. Each female connector has a corresponding male connector (16), which is inserted in a second PTFE holder (17) secured to the bottom section box. The external shield of each coaxial cable is connected to the ground of the amplifier by means of another male-female connection. This kind of connection allows for electrical continuity from the probe tips to the electronic section, without the need for any cable to pass outside the shielding aluminum boxes. Moreover, the base of the probe system can be easily removed from the bottom section for operating on the electronic section (changing batteries, changing amplifier configuration and so on). Once the base is inserted into the bottom section, electric continuity from the tips to the electronic section is automatically obtained and, at the same time, the electronic section is completely shielded from the environment. At this point one may position the sample holder and contact the DUT pads with the aid of a microscope (not shown in Fig. 1), and, once the contact is made, put the top cover in place thus obtaining a structure in which the sample is shielded from the electronic section and both are completely shielded from the environment, the only electrical connection being the BNC connectors (18) from the output of the noise amplifiers. Since the samples must be glued on top of the sample holder, one may want to use several holders, one for each sample, in order to speed up the sample changing procedure. This operation is quite simple: you just need to remove the top cover, rise the tips, remove one holder, put another in its place, contact the new DUT and put back the top cover for starting another measurement. Note that, of course, also conventional electrical characterization (I-V, C-V) is possible, since one can just use the bottom section as an adapter for connecting standard instrumentation to the probes and hence to the DUT. It must be noted that the small size of the sample chamber helps in reducing the effects of leakage currents caused by moisture, which is quite a serious problem when dealing with biasing currents as low as 1 pA. In fact, a few grams of silica gel are sufficient to dry out the sample chamber in a few minutes after the top cover is put in place.

III. RESULTS

A set of measurements has been performed for testing the prototype of the probe system we have designed and built. As a first step, we evaluated the leakage current when using the probe system for performing I-V characterization. In order to do so, we used a HP4155B Semiconductor Parameter Analyzer. After evaluating the leakage currents of the instrument itself, by leaving the cables disconnected from the probe system, we made the connection to the probe system with the tips not in contact with the sample and we repeated the measurement. In both cases, a voltage step of 30 V was imposed and the evolution of the current was recorded. The results are reported in Fig. 2. Two different components can be observed: a displacement current and a steady state conduction current. As the difference between the two conduction currents is about 200 fA, we conclude that the insulation from one probe to the other is higher than 100 TΩ. As a second step, we performed noise measurements on an n-MOS structure with an oxide thickness of 7 nm, an active area of 10^{-8} m^2 and an n^+ polysilicon gate. A simplified schematics of the circuit we used is reported in Fig. 3. We biased the MOS structure with a constant negative gate voltage by means of a programmable low noise power supply. We evaluated the DC and AC components of the current through the MOS structure by measuring the DC and AC components of the voltage V_u at the output of the transresistance amplifier.

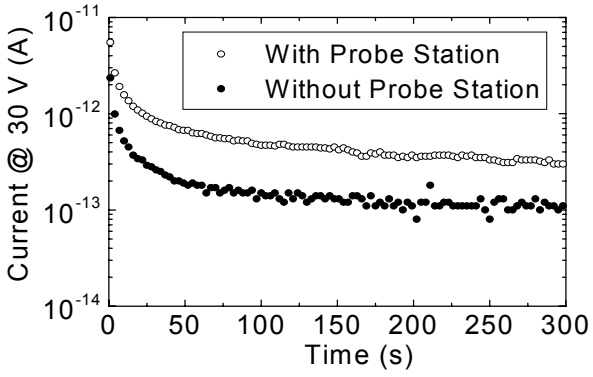

Fig. 2. Evolution of the leakage current at 30 V measured by means of a HP4155B Semiconductor Parameter Analyzer with and without our probe system connected to the instrument. The insulating resistance of the probe system results higher than 100 TΩ.

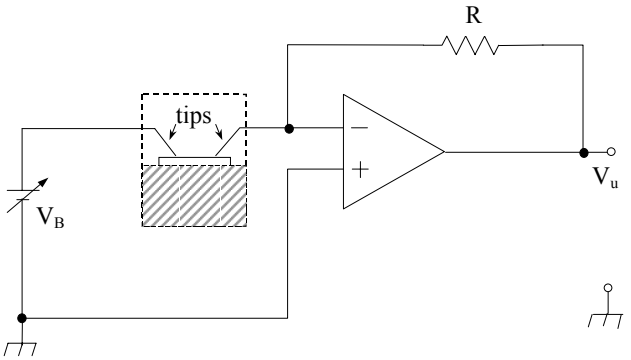

Fig. 3. Circuit configuration used for the low noise measurements in MOS structure.

The results obtained at different DC current levels are shown in Fig. 4 along with the transresistance amplifier background noise. In all the cases, the spectra show a white component at higher frequencies, due to the shot noise associated to the tunneling current. The average value of the difference between this white component and the background noise at frequencies higher than 50 Hz as a function of the DC current level is reported in Fig. 5 along with the straight line corresponding to the theoretical shot noise. The corresponding error, reported in the inset, results less than 5 % in all cases. It is worth noticing that the lowest measured shot noise level is as low as 5.65 fA/√Hz. These results confirm the possibility of performing high sensitivity noise measurements at wafer level. Clearly, further experiments are needed for a complete characterization of our prototype from the point of view of the noise performances. In fact, at lower frequencies and higher DC current levels, a flicker noise component can be observed in Fig. 4.

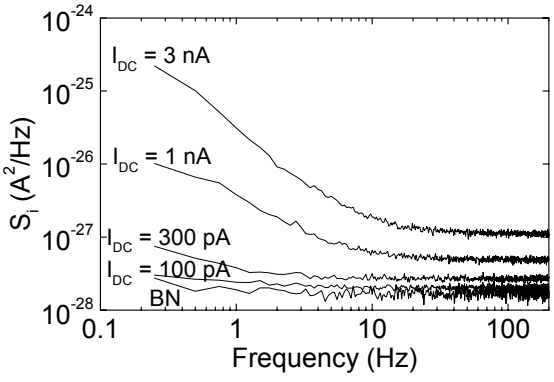

Fig. 4. Power spectral density of the current noise measured in a 7 nm thick oxide MOS structure at different DC current levels. The background noise (BN) of the transresistance amplifier is also shown.

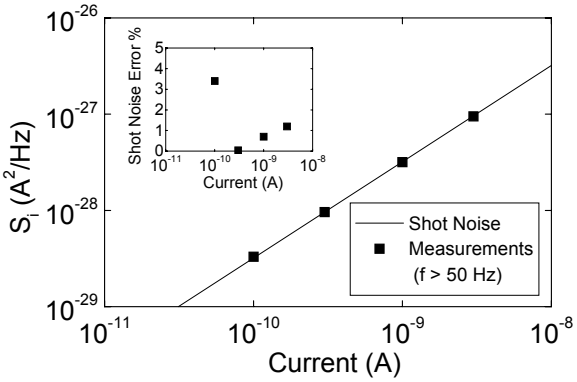

Fig. 5. Average value of the white component observed at frequencies higher than 50 Hz as a function of the DC current value along with the straight line corresponding to the expected shot noise. The error, shown in the inset, is less than 5% in all cases.

Measurements performed on packaged devices confirm that such a noise contribution comes from the DUT. However, an accurate characterization of the contact noise contribution is needed for establishing the ultimate noise performances that can be obtained from our system.

REFERENCES

[1] A. van der Ziel, "Noise: Sources, Characterization, Measurement", Englewood Cliffs, NJ: Prentice-Hall, 1970

[2] G.B. Alers, B.E. Weir, M.A. Alam, G.L. Timp and T. Sorch, "Trap Assisted Tunneling as a Mechanism of Degradation and Noise in 2-5 nm Oxides", *IRPS*, pp. 76-79, 1998

[3] B.Neri, P.Olivo, B.Riccò, "Low-frequency noise in silicon-gate metal-oxide-silicon capacitors before oxide breakdown", *Appl. Phys. Lett.*, vol.51, pp.2167-2169, 1987

[4] F. Crupi, G. Iannaccone, B. Neri, C. Ciofi, S. Lombardo, "Shot Noise Partial Suppression in the SILC Regime", *Microel. Reliab.*, vol. 40, pp. 1605-1608, 2000

[5] K. F. Schuegraf, C. Hu, "Reliability of thin SiO_2", *Semicond. Sci. Technol.,* pp.989-1003,1994